AMENDMENTS TO THE CLAIMS:

This listing of all claims will replace all prior versions, and listings, of claims, in the application.

Listing of Claims:

Claim 1 (currently amended): A membrane switch circuit layout comprising two or more non-conductive membrane layers, each membrane layer having top and bottom surfaces, a conductive circuit trace printed on the top surface of each membrane layer, the [a] first membrane layer being positioned beneath the [a] second membrane layer, the second membrane layer having thru-holes selectively cut there through and positioned to provide electrical connection between circuit traces printed on the membrane layers, pads for receiving conductive ink being printed on the first membrane layer corresponding to the location of the thru-holes in the second membrane layer.

Claim 2 (original): The circuit layout of claim 1 wherein the thru-holes connect the conductive circuit trace printed on the second membrane with the conductive circuit trace printed on the first membrane.

Claim 3 (original): The circuit layout of claim 1 wherein conductive ink at least partially fills the thru-holes.

Claim 4 (original): The circuit of claim 1 wherein the membranes are electrically insulating.

Claim 5 (original): The circuit of claim 1 wherein the second membrane electrically insulates traces printed on its top surface from traces printed on the first membrane.

Claim 6 (original): The circuit of claim 1 further comprising an adhesive positioned between first and second membrane layers.

Claim 7 (original): The circuit of claim 4 wherein the adhesive is selectively printed for openings on the top surface of the first membrane layer.

Claim 8 (original): The circuit of claim 4 wherein the adhesive is selectively printed for openings on the bottom surface of the second membrane layer.

Claim 9 (original): The circuit of claim 4 wherein the adhesive is an adhesive layer positioned between first and second membrane layers, the adhesive layer having openings selectively cut there through.

Claim 10 (canceled).

Claim 11 (original): The circuit of claim 1 wherein the first membrane layer is a film layer between 0.001 and 0.007 inches thick.

Claim 12 (original): The circuit of claim 1 wherein the second membrane layer is a film layer between 0.001 and 0.007 inches thick.

Claim 13 (canceled).

Claim 14 (currently amended): The circuit layout of claim 27 [13], further comprising an adhesive positioned between second and third membrane layers.

Claims 15-26 (canceled).

Claim 27 (new): A membrane switch circuit layout comprising three non-conductive membrane layers, each membrane layer having top and bottom surfaces, a conductive circuit trace printed on the top surface of each membrane layer, the first membrane

layer being positioned beneath the second membrane layer and the second membrane layer being positioned beneath the third membrane layer, the second and third membrane layer having thru-holes selectively cut there through and positioned to provide electrical connection between circuit traces printed on the membrane layers.

Claim 28 (new): The circuit layout of claim 13, further comprising an adhesive positioned between first and second membrane layers.

Claim 29 (new): The circuit layout of claim 13, further comprising a first adhesive positioned between first and second membrane layers and a second adhesive positioned between second and third membrane layers.

Claim 30 (new): The circuit layout of claim 13, wherein the first and second adhesives are selectively printed for openings on the bottom surface of the second and third membrane layers, respectively.

Claim 31 (new): The circuit layout of claim 13, wherein the adhesive first and second adhesives are adhesive layers positioned between first and second membrane layers and the second and third membrane layers, respectively, the adhesive layers having openings selectively cut there through.

Claim 32 (new): The circuit layout of claim 13, wherein the thru-holes in the second membrane layer connect the conductive circuit trace printed on the second membrane layer with the conductive circuit trace printed on the first membrane layer.

Claim 33 (new): The circuit layout of claim 13, wherein the thru-holes in the third membrane layer connect the conductive circuit trace printed on the third membrane layer with the conductive circuit trace printed on the first membrane layer.

Claim 34 (new): The circuit layout of claim 13, wherein the thru-holes in the third membrane layer and the thru-holes in the second membrane layer connect the conductive circuit trace printed on the third membrane layer with the conductive circuit trace printed on the first membrane layer.

Claim 35 (new): The circuit layout of claim 13, wherein conductive ink at least partially fills the thru-holes.

Claim 36 (new): The circuit layout of claim 13, wherein the membrane layers are electrically insulating.

Claim 37 (new): The circuit layout of claim 13, wherein the second membrane layer electrically insulates traces printed on its top surface from traces printed on the first membrane layer and the third membrane layer electrically insulates traces printed on its top surface from traces printed on the second membrane layer.

Claim 38 (new): The circuit layout of claim 13, wherein pads for receiving conductive ink are printed on the first membrane layer corresponding to the location of the thru-holes in the second membrane layer and pads for receiving conductive ink are printed on the second membrane layer corresponding to the location of the thru-holes in the third membrane layer.

Claim 39 (new): The circuit layout of claim 13, wherein the first membrane layer is a film layer between 0.001 and 0.007 inches thick.

Claim 40 (new): The circuit layout of claim 13, wherein the second membrane layer is a film layer between 0.001 and 0.007 inches thick.

Claim 41 (new): The circuit layout of claim 13, wherein the third membrane layer is a film layer between 0.001 and 0.007 inches thick.